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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/592,943	09/15/2006	Hitoshi Saomoto	062998	8662
38834 7590 03/10/2010 WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036				
EXAMINER CARTER, MICHAEL W				
ART UNIT 2828		PAPER NUMBER		
NOTIFICATION DATE 03/10/2010		DELIVERY MODE ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentmail@whda.com

Office Action Summary

Application No.

10/592,943

Applicant(s)

SAOMOTO ET AL.

Examiner

MICHAEL CARTER

Art Unit

2828

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 December 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2, 12 and 13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-2, 12-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/GS/US)
- Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. **Claims 1-2 and 12** remain rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,075,800 (Spear) in view of US Patent 6,618,420 (Gen-Ei) and further in view of US PG Pub 2003/0231685 (Nakamura) according to the previous rejection.
3. **For claims 1 and 12**, Spear teaches a ridge waveguide laser with a ridge (figure 1, label 14) and two supports for protecting the ridge (figure 1, portion of label 10 to right of trough 12 and portion of label 10 to the left of trough 12) and the sidewalls of the support region extend directly downward into an underlying substrate (figure 1, label 11).
4. Gen-Ei teaches placing two lasers (figure 3a, labels 40 and 41) side by side with an isolation groove between them and on the outside edges, which extends into a substrate (label 10) in order to form a multi-beam laser (abstract).
5. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form two of the lasers taught by Spear side by side as taught by Gen-Ei in order to form a multi-beam laser.
6. The above combination teaches a plurality of ridges (Spear, label 14 from 1st and second laser) arranged in parallel with each other (Gen-Ei figure 5B) inside a pair of first supports protecting said ridges (Spear, figure 1, label 10 outside trough 12,

supports on the outside edge of each laser); a pair of second supports provided between said plurality of ridges and protecting said ridges (Spear, figure 1, label 10 outside trough 12, support on the inside edge of each laser); a monitor region provided to the outermost edge of said semiconductor laser element (Gen-Ei, figure 3a, groove on outside edge of laser 41) and wherein sidewalls of said second supports (Spear, figure 1, sides of laser) extend directly downward into an underlying substrate (Spear, label 11) forming a second isolation groove (Gen-Ei groove between lasers 40 and 41) between said adjacent sidewalls. The combination further teaches the electrodes are formed on each ridge (Spear, electrode 15 covers ridge 14, while Gen-Ei teaches placing two such lasers side by side).

7. While the combination does not explicitly teach the monitor region is to monitor progress of the etching and serves as an isolation groove, this recites an intended use which does not distinguish the structure from the prior art.

8. The combination does not teach a ratio of an area of said first and second supports relative to an area of said semiconductor laser element is set within a range from more than 33% to less than 52%.

9. However, Nakamura does teach a ratio of an area of said first and second supports (figure 2, portion of W outside trenches 15) relative to an area of said semiconductor laser element (defined in figure 2 by the width W) is set within a range from more than 33% to less than 52% (paragraph 73 teaches the width W in figure 2 is 30-40 μm while the grooves 15 are 10 μm and the wave guide is 2 μm the supports are therefore 4-9 μm each. The supports and laser have the same length, so when

considering the ratio of the areas of the first and second supports to an area of said laser one must only consider the widths. The total width of the first and second support is 18 μm while the width of an area of said semiconductor laser element is 40 μm . $18/40=.45$ in order to provide a laser capable of high speed performance (abstract). Nakamura also teaches the electrode (figure 2, label 25) is formed over the ridge of the laser (label 16).

10. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the dimensions taught by Nakamura with the previous combination in order to provide a laser capable of high speed performance.

11. Further, Spear teaches the supports are used to provide a thermal conduction path as well as mechanical stability between the chips and substrate (column 2, lines 23-25).

12. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to balance the size of the supports in order provide sufficient thermal conduction (See, for example, US PG Pub 2002/0024985 paragraph 23.) while maintaining sufficient high speed operations since a change in size is generally considered within the ordinary skill in the art.

13. **For claim 2**, the combination teaches each support of the pair of second supports is provided corresponding to each ridge. Each ridge (Spear, label 14) corresponds to a second support (support portion of label 10 for each laser between the ridges).

14. **Claims 13** remains rejected under 35 U.S.C. 103(a) as being unpatentable over

Spear in view Gen-Ei and Nakamura and further in view of US Patent 6,199,561 (Mitsuhashi) according to the previous rejection.

15. **For claim 13**, the combination of Spear, Gen-Ei and Nakamura teaches arranging a plurality of ridges in parallel with each other on an element surface (Gen-Ei, figure 3A, label 10) and providing each ridge with a plurality of supports to sandwich each ridge as discussed in the rejection of claim 1 above providing a block layer on surfaces of said ridges and said supports (Spear, figure 1, label 16) and providing an electrode layer covering the ridges (label 15).

16. Spear does not detail that the patterning (leaving the top of ridge 14 exposed to electrode 15) includes applying a protective film by spin coating to a surface of said block layer; removing said protective film covering a top surface of said ridges; with said protective film serving as a mask.

17. However Mitsuhashi teaches the steps of applying a protective film by spin coating to a surface of a layer; removing said protective film covering a top surface of a selected area; with said protective film serving as a mask are well known in the art for producing semiconductor devices (column 1, lines 14-24).

18. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use Mitsuhashi method of patterning for the patterning required in the method of the previous combination.

Response to Arguments

19. Applicant's arguments filed 12/17/2009 have been fully considered but they are not persuasive.

20. The applicant argues that "an area of said semiconductor laser element" is proportional to the chip width. While the examiner agrees that one particular area of said semiconductor laser element is proportional to the chip width, there are many other possibilities for "an area of said semiconductor laser element," and the applicant does not claim the specific area described on page for of the arguments. For instance "an area" may include only the first support, only the second support, or only the ridge to name three possible examples. In the case of Nakamura, the examiner has chosen an area with the width W in figure 2 which includes 2 supports, two trenches, and the ridge.

21. The applicant further argues that Nakamura's width W does not include an electrode on the ridge; however, electrode 25 clearly covers the ridges as shown in figure 2. The applicant argues on page 5 that the width W is only part of "an area," but as previously discussed, "an area" is not limiting to, for example, the entire width of an element. The applicant further argues, on page 6, that electrodes 25 and 26 correspond to "supports." While that may be a reasonable interpretation, they are at least third and fourth supports which are not required by the previous combination, nor are they required to obtain the benefit of the width, W, taught by Nakamura. These additional areas were, therefore, not used in the calculation of the ratio in the rejection of claim 1 above.

22. As to the motivation to combine, argued by the applicant on page 6, the applicant acknowledges that the shortening of the width W, in Nakamura, causes reduced capacitance. Nakamura also provides suitable dimensions to obtain the reduced W as discussed in the rejection above. It is the reduced capacitance that then allows high speed capacity referred to in the rejection of claim 1 above.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Carter whose telephone number is (571) 270-1872. The examiner can normally be reached on Monday-Friday, 7:00 a.m.-4:30 p.m., EST.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

/Minsun Harvey/
Supervisory Patent Examiner, Art Unit 2828